HIGH POWER PIN DIODE SWITCH MATRIX

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Abstract

A single pole, fifty six throw PIN diode switch matrix has been designed for a G-Band cylindrical steerable beam antenna for the AN/USW-3(V) Integrated Target Control System. Bandwidth of the matrix is 20 percent, and CW power handling capability is greater than one-half kilowatt.

Introduction

A cylindrical array antenna providing a multiplicity of beam positions and a symmetrical electronic switching system for selection of the desired beam position forms an effective means for transmitting to any specified direction around the horizon. The antenna and switches described herein are being developed for the AN/ASW-35 Airborne Drone Control Station (part of the AN/USW-3(V) System) that controls several remotely controlled vehicles by communicating with them sequentially. Since the locations of the vehicles are not restricted with respect to the command system, complete flexibility and rapid steering are required.

Antenna System

The array and switching arrangement are shown in simplified form by Figure 1. In addition to the array and switches, the antenna includes a lens which accepts the signal from the transmitter and divides it into a number of individual signals to be applied to the various active radiating elements. These signals have the proper magnitudes and phases to generate a focussed beam when radiated into space by the elements. The inverse operations occur by reciprocity when the antenna is receiving an incoming signal.

Lens

In the present system, the lens is built in the form of two flat parallel metal disks joined around their edges by a metal ring to form a closed waveguide region. A series of probes fitted with connectors for coaxial cables is placed around the perhiphery of the lens. When a signal is applied to one of these terminals, the energy travels across the lens as a TEM wave and excites a group of probes on the opposite side of the lens. Cables then conduct these signals to a group of radiating elements. To obtain the proper element phasing, the diameter of this flat plate lens is made equal to half the diameter of the array and the number of terminals is made equal to half the number of radiating elements. A two-throw switch is provided for each lens terminal to connect it to either one of two diametrically opposite elements. A two-throw switch is also provided for each lens terminal to connect it to either the transmitter or a radiating element as required.

Beam Steering

If only one lens terminal were used as an input at any instant, the number of available discrete beam positions would be the same as the number of radiating elements. However, in the present system, the lens terminals are used in pairs, and intermediate beam positions are generated by varying the relative excitations of the adjacent terminals. Consequently, the system includes two identical switch matrixes, one connected to the odd-numbered terminals and the other connected to the even-numbered terminals. The inputs to the two matrixes are connected to the outputs of a variable power divider. The beam steering process thus includes a coarse steering step, which consists of selecting the appropriate lens terminals, and a fine steering step, which consists of setting the power divider to the proper power ratio.

The fine steering process determines the relationship between the diameter of the array and the number of radiating elements placed around its periphery since the adjacent beams must "cross-over" at the proper level. For the cylindrical geometry, the required spacing between elements works out to be approximately one-half wavelength. In the present antenna, system requirements, physical size limitations, and other considerations led to a choice of 216 as the number of radiating elements. As a result, the lens has 108 terminals, and the odd and even switch matrixes each have 54 outputs.

Switch Matrix

There are several possible ways to assemble such a matrix, and various combinations of two-, three-, and four-throw single junction switches have been considered. The development program has shown however, that two-throw switches perform so much better than switches with more outputs that the present design uses two-throw elements to make up the required 54-throw matrix. Each matrix is being constructed as a central module with seven outputs surrounded by seven modules having eight outputs each. This gives 56 outputs, of which two are not used. Each module consists of three levels of two-throw switches in cascade, and in the case of the seven-throw module, one of the eight possible outputs is not used. The existence of unused outputs may seem wasteful, but this is more than compensated for by the commonality of design throughout the system.

The maximum power the antenna can handle is limited by the PIN diodes used in the switching matrix. Therefore, to increase the power handling capability of the antenna it is necessary to increase the power handling of the diodes.

Pin Diodes

The parasitic parameters of conventional packages tend to narrow the usable bandwidth of a diode and also increase the dissipation in the chip. Standard low parasitic packages have a Kovar lead which is unplated in the area of the glass feed through. This magnetic lead cannot handle sufficient current to be used in high power applications. This has been verified experimentally. These leads have melted while passing 300 watts at 4.6 GHz in a 50 ohm PTFE-Glass stripline test fixture. An analysis showed that gold has 167 times lower resistance to a 4.5 GHz signal than Kovar. Using this as a guide, a low parasitic package was designed which uses 0.050 inch wide gold leads that are 0.005 inch thick. This package passed 600 watts at 4.6 GHz.

The choice of chips to place in this package was not straightforward. The analysis of the forward biased diode indicates the need for a diode with very low series resistance. However, the analysis of the reversed biased diode indicated the need for a low capacitance diode. High power tests at 4.6 GHz demonstrated that a 0.5 pF, 0.5 ohm diode could hold off the equivalent of 600 watts but failed to pass 600 watts. A 0.25 pF, 1.0 ohm diode passed 600 watts, but could hold off only the equivalent of 200 watts. It is easier to parallel two diode chips and maintain low thermal resistance than it is to series them. Therefore, two, 0.25 pF, 1.0 ohm diode chips are paralleled in a low, parasitic, diode package. The net thermal resistance of these chips was consistently less than $3^{o}C/W$ at $25^{o}C$.

SP2T Switch Design and Performance

The circuit design of the SP2T switch with diode spaced $\lambda/4$ from the pole of the switch was accomplished using a computer optimization program. Inputs to the program included the packaged diode S-parameters in the forward and reverse bias states and proposed circuit configuration. The optimization process resulted in an SP2T switch design with a theoretical maximum insertion loss of 0.3 dB over a 20 percent bandwidth at G-band. The maximum predicted vswr over the same bandwidth was 1.3:1.

The biasing scheme for the switch matrix has the center conductor serving as the common bias return for all diodes, thus eliminating a potential power disispation problem by not requiring dc blocking capacitors in the stripline center conductor. Capacitance required for the broadband rf bypass is achieved by using a thin coat of Astrodyne No. 922*, (a high thermal conductivity epoxy paint) between the diode case and switch chassis. The dielectric medium for the stripline switch is PTFE-Glass, and the ground plane spacing is 0.25 inch.

The maximum insertion loss measured at 1.0 milliwatt for a SP2T switch is 0.4 dB over a 20 percent bandwidth at G-band. Approximately 40 percent of the loss is in each diode and the reamining 20 percent is in the other circuitry. Maximum vswr is 1.3:1 and minimum isolation is 25 dB.

High Power Test and Analysis

A high power test of the SP2T switch was conducted. The results of the test are shown in Figure 2 and indicate a maximum temperature rise of 140°C for either diode bias state. This is significantly higher than the 65°C which is predicted by using the thermal resistance measured at 25°C and the loss measured with low power. More significantly the entire curve of temperature versus input power is nonlinear. This nonlinear relationship can be explained by considering both the power dissipation and thermal resistance as a function of junction temperature.

Power Dissipation

The power dissipation of a reversed biased diode was measured as a function of temperature and is plotted in Figure 3. A linear equation approximates these points and is given as equation 1. The measured points were obtained by placing three diodes in a fixture measuring the total change and dividing by three. Fixture losses and mismatch losses were accounted for at each temperature.

$$P_{dis} = P_{in}\left[\frac{T_j - 200}{175}(.021) + .066\right] \text{ watts} \qquad (1)$$

Thermal Resistance

The thermal resistance of the diode from junction to case is comprised of two components, the thermal resistance of the silicon and the thermal resistance of the die bond. It has been reported that the thermal conductivity varies with temperature.(1) This data has been replotted in the form of thermal resistivity (R) in Figure 4. Equation 2 is a close approximation to these data points over the 25°C to 200°C temperature range.

$$R = \frac{T + 169}{584} \quad \frac{^{o}C - in}{W} \qquad (2)$$

For simplicity, assume the thermal model of the diode is a length (L) of silicon equal to the thickness of the chip and an area (A) nearly equal to that of the two chips in parallel. With these assumptions, the thermal resistance of the silicon is calculated and given by equation 3.

$$\theta_{si} = \frac{RL}{A} = .0103\ T_j + 1.75\ \frac{^{o}C}{W} \qquad (3)$$

This is the same as equation 2 except for a scale change. This equation is valid because the actual area of the silicon is greatly reduced toward the top of the chip but the length of the path is also reduced because the heat source is not at the very top of the chip. The total thermal resistance of the diode includes the effect of equation 3 and also the bond resistance. Measured thermal resistance is also plotted in Figure 4.

Note that equation 3 can be made to be a resonable fit to the measured data by adding a constant of 0.5 °C/W. This constant should be considered to be the thermal resistance of the die bond. The resulting equation defining the relationship between diode junction to case thermal resistance (θ_{jc}) and temperature is given as equation 4.

$$\theta_{jc} = .0103\ T_j + 2.25\ \frac{^{o}C}{W} \qquad (4)$$

Temperature rise is the product of thermal resistance and power dissipation, hence equation 5 is the product of equations 1 and 4.

$$T_j - T_o = P_{in}\left[\frac{T_j - 200}{175}(.021) + .066\right]\left[.0103\ T_j + 2.25\right]\ ^{o}C \qquad (5)$$

This is plotted in Figure 2.

The preceding analysis has been for a reverse biased diode. A similar analysis can be done for a forward biased diode.

SP7T Switch

Figure 5 shows a breadboard of an SP7T switch with the cover and top dielectric removed. This switch is essentially an SP8T except with one unused port. Measured results of this switch are given in Figure 6. The loss data includes the loss of several inches of stripline needed to position the input and output terminal at the required locations.

Conclusions

Antennas can be built with 360 degrees of electronic scan that will handle more than one-half kilowatt of average power. A low parasitic diode package was developed which will handle high average power. It has also been shown that high power diodes have a nonlinear temperature rise as a function of power. This nonlinear effect must be accounted for when predicting junction temperature.

References

(1) A. Goldsmith, H. J. Hirchhorn, T. E. Waterman, "Thermophysical Properties of Solid Materials", Armour Research Foundation, WADC Technical Report 58-476, Volume V Appendix pp I-S-3, Nov. 1960.

Acknowledgement

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*Manufactured by Astrodyne, Inc., Wilmington, Massachusetts

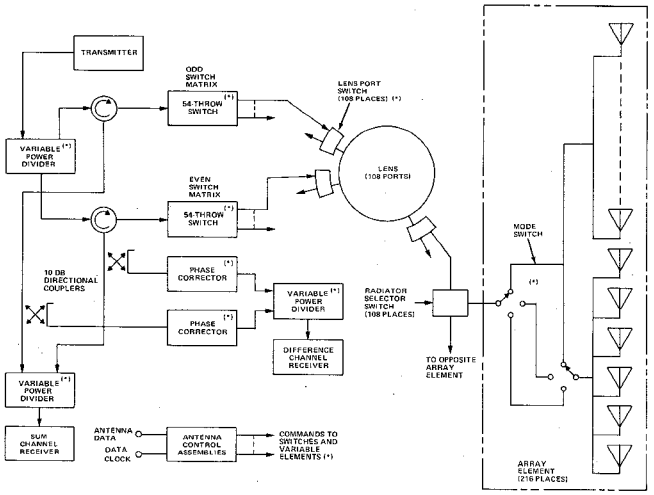

Fig. 1. Antenna system block diagram

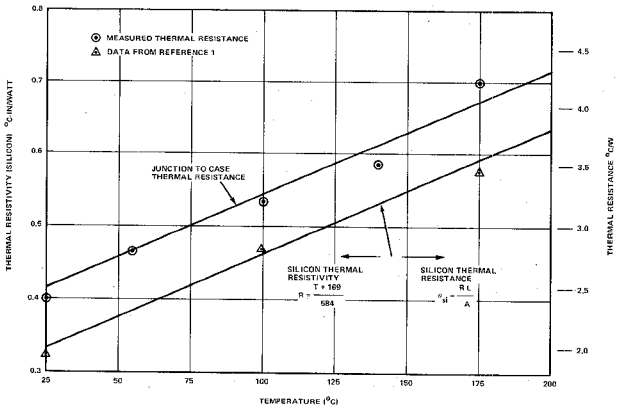

Fig. 4. Thermal resistance

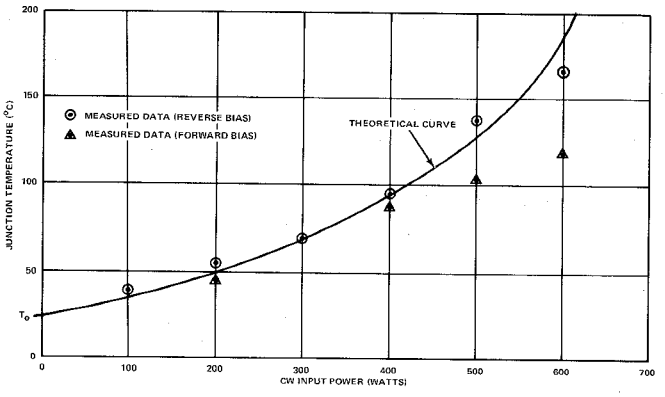

Fig. 2. Junction temperature versus input power

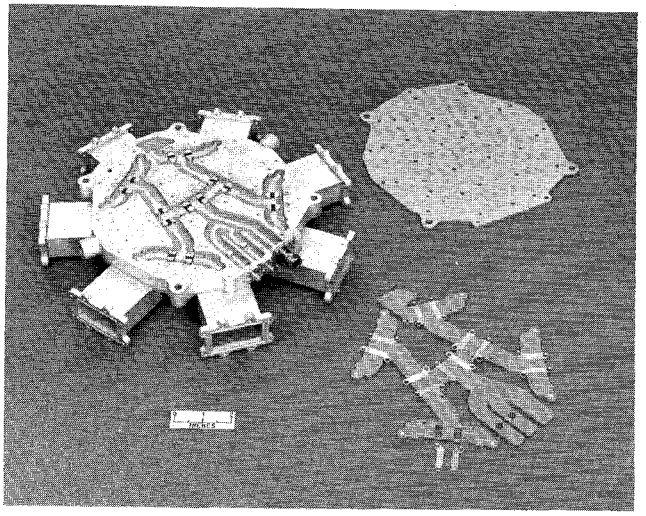

Fig. 5. Breadboard SP7T switch

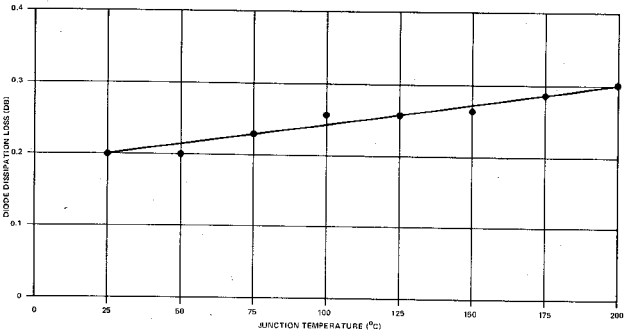

Fig. 3. Diode power dissipation versus junction temperature

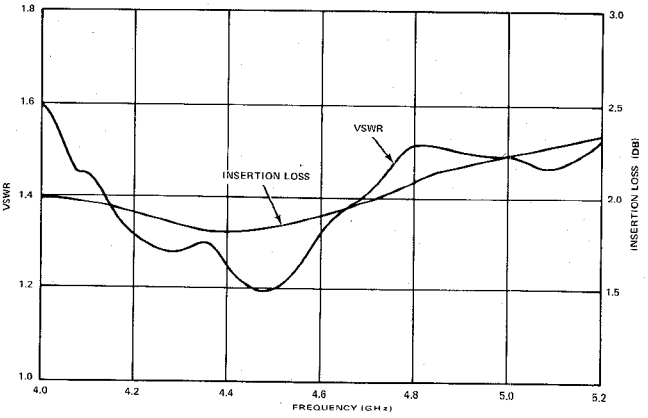

Fig. 6. Breadboard SP7T switch performance